ATSC Digital Television Standard – Part 2: RF/Transmission System Characteristics

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The Advanced Television Systems Committee, Inc., is an international, non-profit organization developing voluntary standards for digital television. The ATSC member organizations represent the broadcast, broadcast equipment, motion picture, consumer electronics, computer, cable, satellite, and semiconductor industries.

Specifically, ATSC is working to coordinate television standards among different communications media focusing on digital television, interactive systems, and broadband multimedia communications. ATSC is also developing digital television implementation strategies and presenting educational seminars on the ATSC standards.

ATSC was formed in 1982 by the member organizations of the Joint Committee on InterSociety Coordination (JCIC): the Electronic Industries Association (EIA), the Institute of Electrical and Electronic Engineers (IEEE), the National Association of Broadcasters (NAB), the National Cable Telecommunications Association (NCTA), and the Society of Motion Picture and Television Engineers (SMPTE). Currently, there are approximately 140 members representing the broadcast, broadcast equipment, motion picture, consumer electronics, computer, cable, satellite, and semiconductor industries.

ATSC Digital TV Standards include digital high definition television (HDTV), standard definition television (SDTV), data broadcasting, multichannel surround-sound audio, and satellite direct-to-home broadcasting.

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1. SCOPE

This Part describes the characteristics of the RF/Transmission subsystem, which is referred to as the VSB subsystem, of the Digital Television Standard. The VSB subsystem offers two major modulation methods: a terrestrial broadcast method (8-VSB), and a high data rate method (16-VSB). These are described in separate sections of this document.

The 8-VSB modulation method is further defined by a set of required elements. Payload data is protected by the Forward Error Correction (FEC) system and is sent using mandatory training sequences. The system described herein also serves as a foundation upon which enhancements can be built and provides signaling of their presence.

2. REFERENCES

At the time of publication, the editions indicated were valid. All referenced documents are subject to revision, and users of this Standard are encouraged to investigate the possibility of applying the most recent edition of the referenced document.

2.1 Normative References

The following documents, in whole or in part, as referenced in this document, contain specific provisions that are to be followed strictly in order to implement a provision of this Standard.

[1] ISO: "ISO/IEC IS 13818-1:1 2007 (E), International Standard: Information technology – Generic coding of moving pictures and associated audio information: systems."

2.2 Informative References

The following documents contain information that may be helpful in applying this Standard.

[2] ATSC: "ATSC Standard for Transmitter Synchronization," Doc. A/110:2011, Advanced Television Systems Committee, Washington, D.C., 8 April 2011.

[3] SMPTE: "Synchronous Serial Interface for MPEG-2 Digital Transport Stream," Doc. ST 310-2010, Society of Motion Picture and Television Engineers, White Plains, N.Y., 2010.

[4] ATSC: "Digital Television Standard, Part 3 – Service Multiplex and Transport Subsystem Characteristics," Doc. A/53, Part 3:2009, Advanced Television Systems Committee, Washington, D.C., 7 August 2009.

[5] ATSC: "Digital Television Standard, Part 1 – Digital Television System," Doc. A/53, Part 1:2007, Advanced Television Systems Committee, Washington, D.C., 7 August 2009.

[6] ITU: "Digital multi-programme systems for television, sound and data services for cable distribution," Doc. ITU-T J.83.

3. DEFINITION OF TERMS

With respect to definition of terms, abbreviations, and units, the practice of the Institute of Electrical and Electronics Engineers (IEEE) as outlined in the Institute's published standards [1] shall be used. Where an abbreviation is not covered by IEEE practice or industry practice differs

from IEEE practice, the abbreviation in question will be described in Section 3.3 of this document.

3.1 Compliance Notation

This section defines compliance terms for use by this document:

shall – This word indicates specific provisions that are to be followed strictly (no deviation is permitted).

shall not – This phrase indicates specific provisions that are absolutely prohibited.

should – This word indicates that a certain course of action is preferred but not necessarily required.

should not – This phrase means a certain possibility or course of action is undesirable but not prohibited.

3.2 Treatment of Syntactic Elements

This document contains symbolic references to syntactic elements used in the audio, video, and transport coding subsystems. These references are typographically distinguished by the use of a different font (e.g., restricted), may contain the underscore character (e.g., sequence_end_code) and may consist of character strings that are not English words (e.g., dynrng).

3.2.1 Reserved Elements

One or more reserved bits, symbols, fields, or ranges of values (i.e., elements) may be present in this document. These are used primarily to enable adding new values to a syntactical structure without altering its syntax or causing a problem with backwards compatibility, but they also can be used for other reasons.

The ATSC default value for reserved bits is '1.' There is no default value for other reserved elements. Use of reserved elements except as defined in ATSC Standards or by an industry standards setting body is not permitted. See individual element semantics for mandatory settings and any additional use constraints. As currently-reserved elements may be assigned values and meanings in future versions of this Standard, receiving devices built to this version are expected to ignore all values appearing in currently-reserved elements to avoid possible future failure to function as intended.

3.3 Acronyms and Abbreviation

The following acronyms and abbreviations are used within this document.

16-VSB -16 level Vestigial Sideband

8-VSB – 8 level Vestigial Sideband

DFS – Data Field Sync

ECC – Error Correction Code

$\mathbf{f_{frame}}$ – Data frame rate

$\mathbf{f_{seg}}$ – Data segment rate

FEC – Forward Error Correction

MPEG – Moving Pictures Experts Group

MUX – multiplexer

PCR – Program Clock Reference

PRBS – Pseudo random binary sequence

RS – Reed-Solomon (error correction coding)

S_r – Symbol rate

T_r –- Transport bit rate

TS – Transport Stream

VSB – vestigial sideband modulation

3.4 Terms

The following terms are used within this document.

Data Field – A sequence of 313 Data Segments of which the first is a Data Field Sync Data Segment.

Data Field Sync – A Data Segment that carries information necessary to identify the framing structure of the VSB signal and that carries data useful in recovering the signal.

Data Segment – A data structure comprising four segment sync symbols and 828 data symbols.

Data Segment Sync – A four-symbol sequence that identifies the start of a Data Segment.

reserved – An element that is set aside for use by a future Standard.

4. SYSTEM OVERVIEW

A basic block diagram representation of the system is shown in Figure 4.1. According to this model, the digital television system can be seen to consist of three subsystems.

- Source coding and compression
- Service multiplex and transport
- RF/transmission

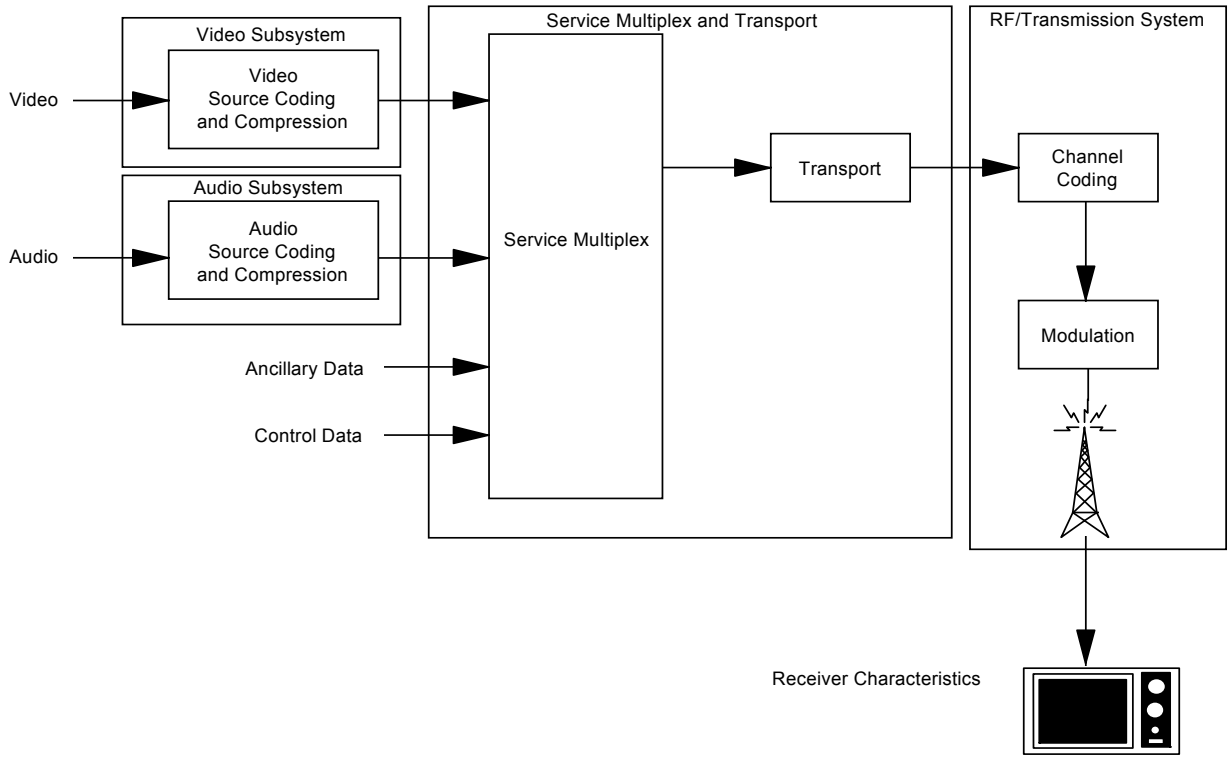


Figure 4.1 ITU-R digital terrestrial television broadcasting model.

This Part documents the requirements for the block labeled "RF/Transmission System" shown in Figure 4.1.

5. TRANSMISSION CHARACTERISTICS FOR TERRESTRIAL BROADCAST

The terrestrial broadcast mode (known as 8-VSB) delivers an MPEG-2 Transport Stream (MPEG-2-TS) at rate T_r (approximately 19.39 Mbps) in a 6 MHz channel.[1]

See Figure 5.1[2] for the functional block diagram. Incoming data is randomized and then encoded using Reed-Solomon (RS) coding for forward error correction (FEC), one-sixth-Data-Field interleaving and two-thirds-rate trellis coded modulation. The randomization and FEC processes are not applied to the sync bytes of the transport packets, which are represented in transmission by Data Segment Sync signals. Following randomization and forward error correction processing, the data packets are formatted into Data Frames for transmission, and Data Segment Sync and Data Field Sync are added. The signal is modulated and a small pilot carrier is inserted prior to RF up-conversion.

[1] See Section 8.2 of [4] for the exact bit rate of the MPEG-2 Transport Stream.

[2] Note that the optional pre-equalizer and RF up-converter blocks are implementation dependent and not addressed in this Part.

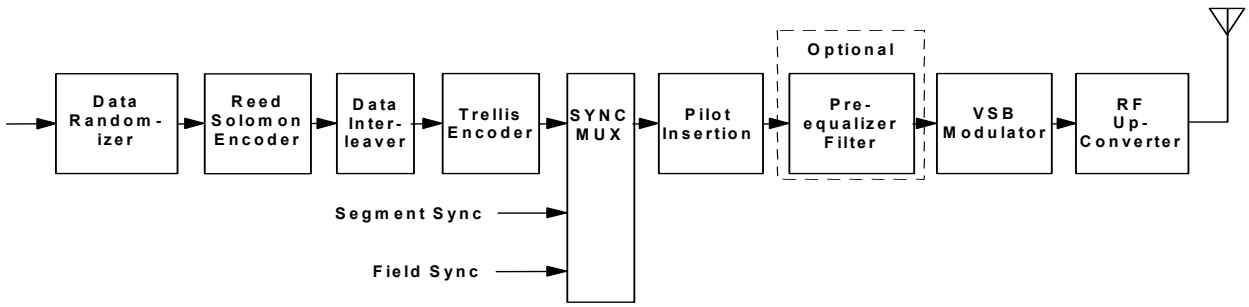


Figure 5.1 Functional block diagram.

5.1 Data Organization

Figure 5.2 shows how the data are organized for transmission. Each Data Frame consists of two Data Fields, each containing 313 Data Segments. The first Data Segment of each Data Field is a unique synchronizing signal (Data Field Sync) and includes the training sequence used by the equalizer in the receiver. The remaining 312 Data Segments each carry the equivalent of the data from one 188-byte transport packet plus its associated RS-FEC overhead.

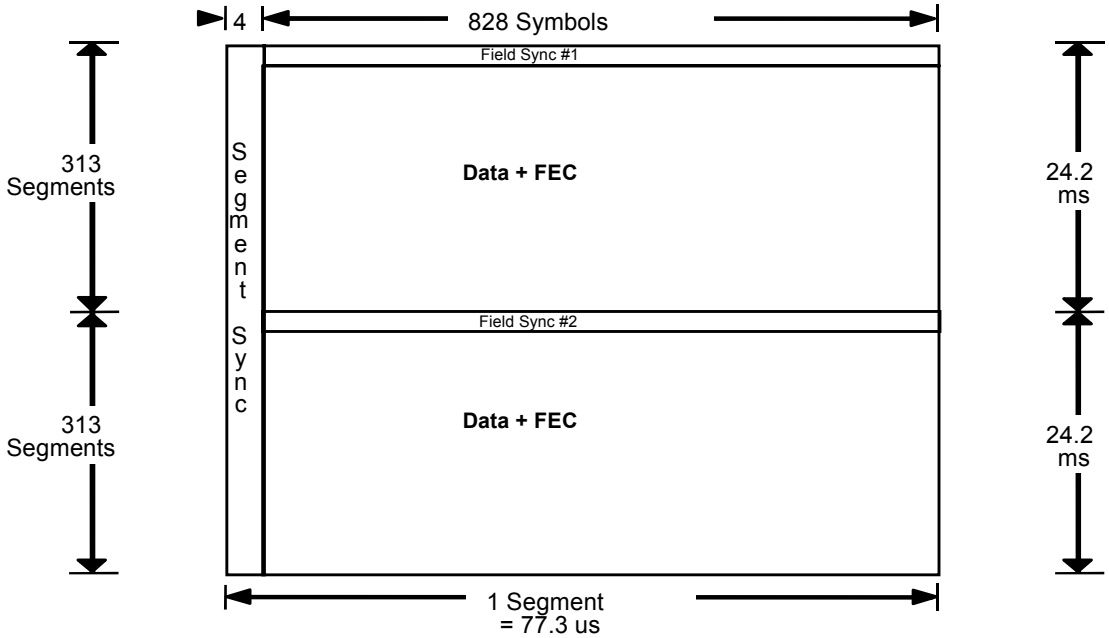


Figure 5.2 VSB data frame without extra field sync.

The actual data in each Data Segment comes from several transport packets because of data interleaving. Each Data Segment consists of 832 symbols. The first 4 symbols are transmitted in binary form and provide segment synchronization. This Data Segment Sync signal also represents the sync byte of the 188-byte MPEG-2-compatible transport packet. The remaining 828 symbols of each Data Segment carry data equivalent to the remaining 187 bytes of a transport packet and its associated RS-FEC overhead. These 828 symbols are transmitted as 8-level signals and therefore carry three bits per symbol. Thus, 828 x 3 = 2484 bits of data are

carried in each Data Segment, which exactly matches the requirement to send a protected transport packet:

187 data bytes + 20 RS parity bytes = 207 bytes

207 bytes x 8 bits/byte = 1656 bits

Two-thirds rate trellis coding requires 3/2 x 1656 bits = 2484 bits

The exact symbol rate shall be as given by Equation 1 below:

(1) Sr (MHz) = 4.5/286 x 684 = 10.76... MHz

The resulting frequency of a Data Segment is given in Equation 2 below:

(2) fseg = Sr / 832 = 12.94... X 103 Data Segments/s

The resulting Data Frame rate is given by Equation (3) below:

(3) frame = fseg/626 = 20.66 ... frames/s

The symbol rate S_r and the transport rate T_r shall be locked to each other in frequency.[3]

5.2 Error Protection

Terrestrial broadcast mode error protection consists of data randomizing, concatenated RS encoding, convolutional byte interleaving, and trellis coding and intrasegment symbol interleaving.

5.2.1 Data Randomizing

A data randomizer shall be used on all input data to randomize the data payload. The data randomizer XORs all the incoming data bytes with a 16-bit maximum length pseudo random binary sequence (PRBS) which is initialized at the beginning of the Data Field. The PRBS is generated in a 16-bit shift register that has 9 feedback taps. Eight of the shift register outputs are selected as the fixed randomizing byte, where each bit from this byte is used to individually XOR the corresponding input data bit. The data bits are XORed MSB to MSB ... LSB to LSB.

The randomizer generator polynomial is as follows:

$$G_{(16)} = X^{16} + X^{13} + X^{12} + X^{11} + X^{7} + X^{6} + X^{3} + X + 1$$

The initialization (pre-load) to 0xF180 (load to 1) occurs during the Data Segment Sync interval prior to the first Data Segment.

The randomizer generator polynomial and initialization is shown in Figure 5.3.

[3] As described in Part 3 of A/53[4] Section 8.2.

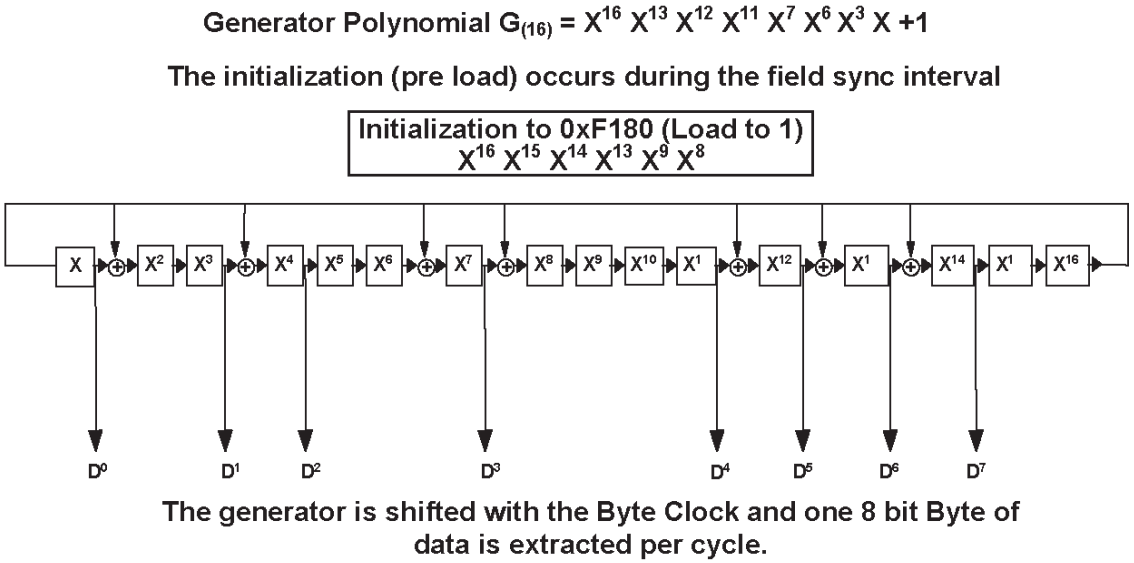


Figure 5.3 Randomizer polynomial.

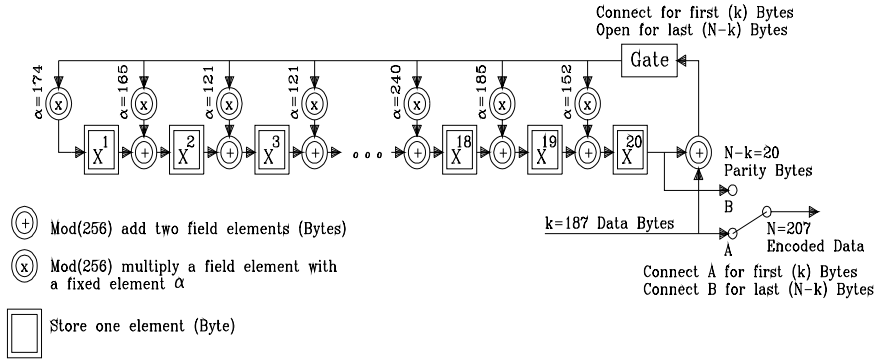
5.2.2 Reed-Solomon Encoding

The randomizer output is the input for the RS Encoder. The RS code used in the VSB transmission subsystem shall be a t = l0 (207,187) code. The RS data block size is 187 bytes, with 20 RS parity bytes added for error correction. A total RS block size of 207 bytes is transmitted per Data Segment.

In creating bytes from the serial bit stream, the MSB shall be the first serial bit. The 20 RS parity bytes shall be sent at the end of the Data Segment. The parity generator polynomial and the primitive field generator polynomial are shown in Figure 5.4.

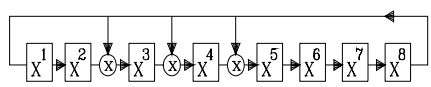
$$\prod_{i=0}^{i=2t-1}(X+\alpha^{i}) = X^{20} + X^{19}\alpha^{17} + X^{18}\alpha^{60} + X^{17}\alpha^{79} + X^{16}\alpha^{50} + X^{15}\alpha^{61} + X^{14}\alpha^{163} + X^{13}\alpha^{26} + X^{12}\alpha^{187} + X^{11}\alpha^{202} + X^{10}\alpha^{180} + X^{9}\alpha^{221} + X^{8}\alpha^{225} + X^{7}\alpha^{83} + X^{6}\alpha^{239} + X^{5}\alpha^{156} + X^{4}\alpha^{164} + X^{3}\alpha^{212} + X^{2}\alpha^{212} + X^{1}\alpha^{188} + \alpha^{190}$$

$$= X^{20} + 152X^{19} + 185X^{18} + 240X^{17} + 5X^{16} + 111X^{15} + 99X^{14} + 6X^{13} + 220X^{12} + 112X^{11} + 150X^{10} + 69X^{9} + 36X^{8} + 187X^{7} + 22X^{6} + 228X^{5} + 198X^{4} + 121X^{3} + 121X^{2} + 165X^{1} + 174$$



Primitive Field Generator Polynomial (Galois Field)

$$G(256) = X^{8} + X^{4} + X^{3} + X^{2} + 1$$



Each shift of the generator produces a field element

Figure 5.4 Reed-Solomon (207,187) t=10 parity generator polynomial.

5.2.3 Convolutional Byte Interleaving

Interleaving in the VSB transmission system is provided to a depth of one-sixth of a Data Field (approximately 4 ms deep). The interleaver employed shall be a 52-data segment (intersegment) convolutional byte interleaver. Only the data bytes of each 208-byte data segment (including the RS parity bytes) shall be convolutionally interleaved; i.e., the sync byte of each segment shall not be interleaved. Due to the RS block length of 207 bytes (resulting from exclusion of the sync byte) and the interleaver segment length of 208 bytes, the positions of successive data segments precess with respect to interleaver operation.

A commutated shift register form of the convolutional data byte interleaver is shown in Figure 5.5. In the commutated shift register form, M is the increment in the number of bytes per row, B is the interleaving degree (the number of rows), and N is the size of the data structure being interleaved. The interleaver parameters shall be M = 4 and B = 52, resulting in N = 208 (MxB).

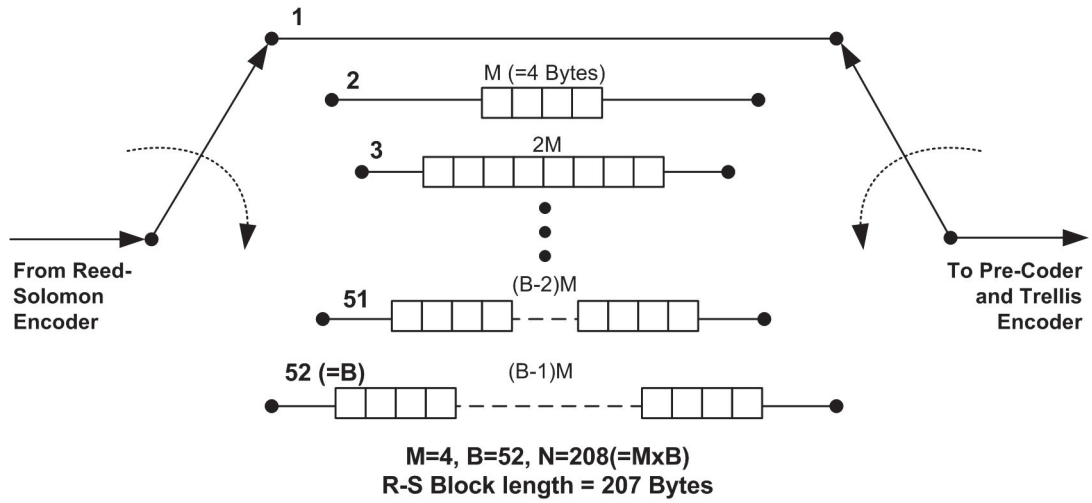


Figure 5.5 Convolutional interleaver (byte shift register illustration).

The byte order of interleaver output shall be the same as that obtained from the shift register form of interleaver shown in Figure 5.5. The interleaver shall be synchronized to the first data byte of the Data Field such that the first byte of the data field has a zero-byte delay. In the commutated shift register form of interleaver, the input and output commutators shall step one position per input/output byte, thereby selecting the same delay path at the same time. The shift register in the selected path shifts once per selection of that path.

5.2.4 Trellis Coding and Intrasegment Symbol Interleaving

Twelve identical trellis encoders shall be used, and their outputs shall be interleaved on an intrasegment basis.

The data processed by each of the twelve trellis encoders shall be encoded using the differential encoder, the 4-state convolutional encoder, and the eight-level symbol mapper shown in Figure 5.6. A two-thirds rate (R=2/3) trellis code is employed. A 4-state optimal Ungerboeck code is used for the encoding. For each trellis encoder, one input bit is encoded into two output bits using a one-half-rate convolutional code while the other input bit is differentially encoded. A differential encoder shall be applied to the MSB of each bit pair (X_2 in Figure 5.6) to produce one output bit (Z_2) as shown in Figure 5.6. The LSB of each bit pair (X_1 in Figure 5.6) shall be convolutionally encoded to produce two output bits (Z_1 and Z_0) as shown in Figure 5.6.

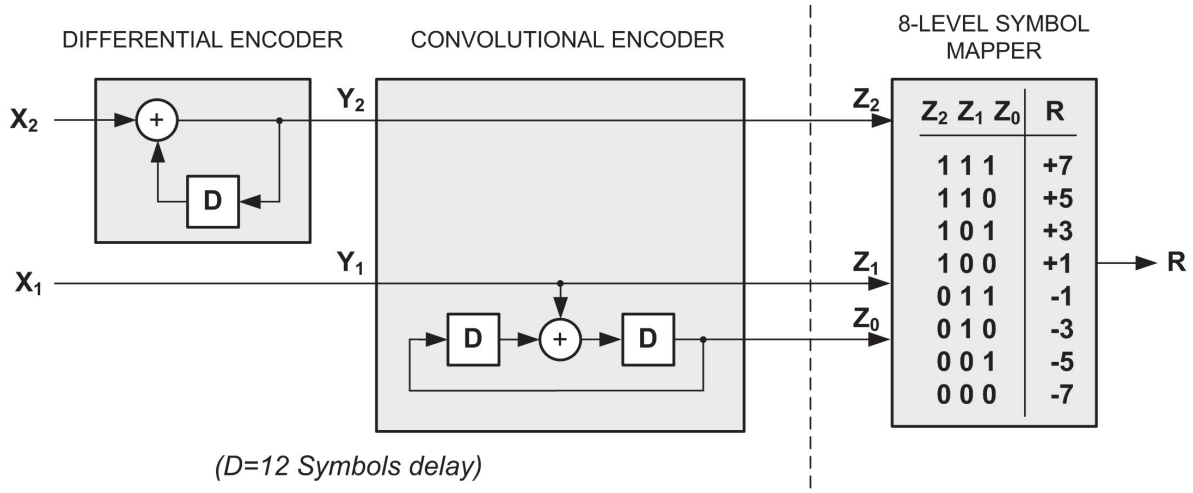


Figure 5.6 Effective single Trellis encoder.

The mapping of the trellis code shall be an 8-level (3-bit), one-dimensional constellation as shown in the 8-Level Symbol Mapper table in Figure 5.6. The transmitted signal is designated 8-VSB.

Each input byte from the convolutional byte interleaver is processed as a whole byte by one of the twelve trellis encoders to produce four output symbols. Bit pairs shall be extracted from each output byte from the convolutional byte interleaver in MSB-to-LSB order: (7,6), (5,4), (3,2), (1,0). As shown in Figure 5.6, the bit pairs are trellis encoded and interleaved on an intrasegment basis, with the MSB of each bit pair (7, 5, 3, 1) differentially encoded and the LSB of each bit pair (6, 4, 2, 0) feedback convolutionally encoded, employing 12-symbol delays "D" in three places. Each 12-symbol delay "D" of Figure 5.6 consists of a one-bit register that is clocked once per output symbol of the Trellis Encoder and therefore once per 12 output symbols of the final multiplexed output of Figure 5.7.

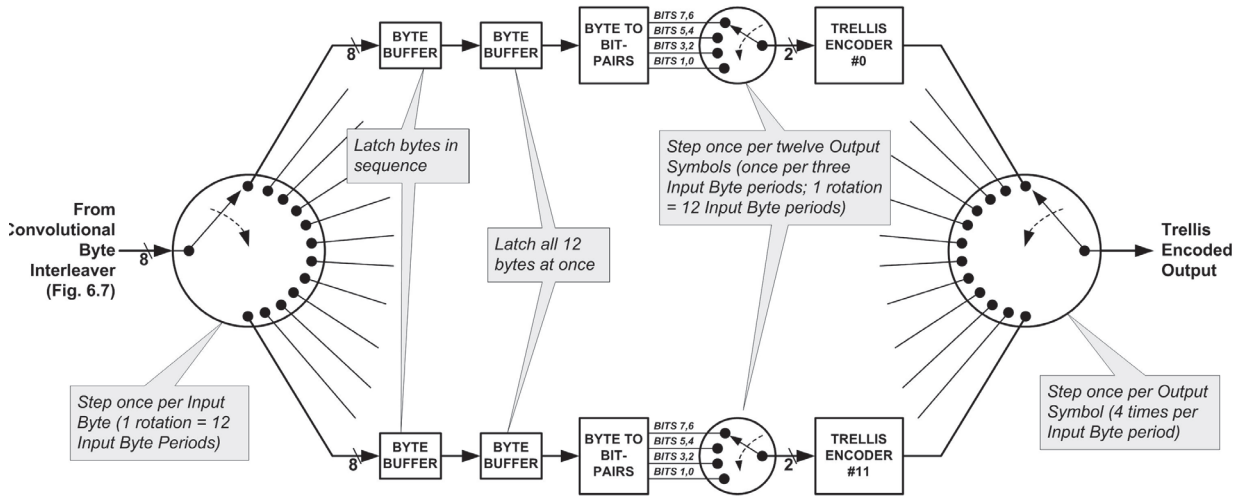


Figure 5.7 Trellis code interleaver.

Intrasegment interleaving surrounding the trellis coding process results in encoding symbols (0, 12, 24, 36 ...) in one encoder, symbols (1, 13, 25, 37, ...) in a second encoder, symbols (2, 14, 26, 38, ...) in a third encoder, and so on for a total of 12 encoders.

The input data to the twelve trellis encoders shall be interleaved by an intrasegment interleaver as shown in Figure 5.7. Sequential data bytes from the convolutional byte interleaver are demultiplexed into the trellis encoders, and each whole byte is processed by one of the twelve trellis encoders. Each byte results in four symbols produced by a single trellis encoder.

The differential encoder and convolutional encoder processes shown to the left of the vertical dashed line in Figure 5.6 are necessarily realized twelve times—once for each of the twelve trellis encoders—due to the requirement for independent memory/delay elements "D" to store the states of the twelve independent encoders. The mapper shown to the right of the vertical dashed line in Figure 5.6 contains no memory elements and therefore need not be realized more than once if it follows the output multiplexer of the intrasegment interleaver.

The input demultiplexer shown (as the left circle) in Figure 5.7 shall send the first byte of the first Data Segment of each Data Field to trellis encoder #0. Successive input bytes of a given Data Segment shall be sent to successive Trellis Encoders; i.e., the demultiplexer steps once per input byte. The data output from the input demultiplexer shall follow normal ordering from encoder 0 through 11 (and repeating) for the first Data Segment of the frame.

The input demultiplexer shall advance by four positions on each segment boundary (corresponding to the Data Segment Sync interval). As a result, the first byte of the second Data Segment is sent to trellis encoder #4, the first byte of the third Data Segment is sent to trellis encoder #8, and so on.

The states of the trellis encoders shall not be advanced during the Data Segment Sync interval.

The output multiplexer shown (as the right circle) in Figure 5.7 shall select the output of trellis encoder #0 for the first symbol of the first Data Segment in a Data Field. The output multiplexer shall advance one position per output symbol until a total of 828 symbols (one Data Segment) has been output.

The output multiplexer shall advance by four positions (i.e., four symbols) on each segment boundary (corresponding to the Data Segment Sync interval).

Due to the advancement of the output multiplexer during Data Segment Sync, the order of output changes for the second segment and symbols are read first from encoders 4 through 11, and then 0 through 3. The third segment reads first from encoder 8 through 11 and then 0 through 7. This three-segment pattern repeats 104 times through the 312 Data Segments of each Data Field.

Table 5.1 shows the interleaving sequence for the first three Data Segments of a Data Field. This three-segment pattern occurs 104 times in each Data Field. In this table, E0 represents a symbol from encoder #0, E1 from encoder #1, etc. The interleaving is such that symbols from each encoder occur at a spacing of twelve symbols. The twelve-symbol spacing between symbols from the same encoder is maintained from one Data Segment to the next Data Segment after the insertion of Data Segment Sync.

After the Data Segment Sync is inserted, the ordering of the data symbols is such that symbols from each encoder occur at a spacing of twelve symbols.

Table 5.1 Symbol Interleaving Sequence for 3-Data-Segment Cycle

Segment	Symbols #0 to #11	Symbols #12 to #23	...	Symbols #816 to #827
0	E0 E1 E2 ... E11	E0 E1 E2 ... E11	...	E0 E1 E2 ... E11
1	E4 E5 E6 ... E3	E4 E5 E6 ... E3	...	E4 E5 E6 ... E3
2	E8 E9 E10 ... E7	E8 E9 E10 ... E7	...	E8 E9 E10 ... E7

Because of the order of byte input and symbol output, a new byte will be delivered from the input demultiplexer to some of the trellis encoders before some or all of the bit pairs of the previous byte have been encoded. Thus, the process generally will require a buffering arrangement, of which there are multiple possible implementations. An example buffering arrangement is shown as part of Figure 5.7. Bytes input to each trellis encoder are double buffered. The first stages of the twelve double buffers latch bytes in sequence as they are received from the input demultiplexer. The second-stage byte buffers latch bytes simultaneously when the correct twelve input bytes are available in the twelve first-stage byte latches.

A complete conversion of parallel bytes to serialized bit pairs takes 828 bytes to produce a total of 6624 bits. Data symbols are created from 2 bits, so a complete conversion operation yields 3312 data symbols, which corresponds to 4 data segments of 828 data symbols each. Note that 3312 data symbols divided by 12 trellis encoders yields 276 symbols per trellis encoder. Also note that 276 symbols divided by 4 symbols per byte yields 69 bytes per trellis encoder in each complete conversion operation (of 4 data segments).

The conversion starts with the first segment of the field and proceeds with groups of 4 segments until the end of the field. 312 segments per field divided by 4 yields 78 conversion operations per field.

Table 5.2 details the byte to symbol conversion and the associated multiplexing of the trellis encoders. Segment 0 is the first segment of a field. The pattern repeats every 12 segments; segments 5 through 11 are not shown. The effects of advancing the input demultiplexer during Data Segment Sync are illustrated in the shaded cells (Segment 1, symbols 24 and 36), where it may be seen that trellis encoder 4 receives bytes 208 and 216 in succession, rather than bytes 208 and 220.

Table 5.2 Byte to Symbol Conversion, Multiplexing of Trellis Encoders

Symbol	Segment 0			Segment 1			Segment 2			Segment 3			Segment 4		
	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits
0	0	0	7,6	4	208	5,4	8	412	3,2	0	616	1,0	4	828	7,6
1	1	1	7,6	5	209	5,4	9	413	3,2	1	617	1,0	5	829	7,6
2	2	2	7,6	6	210	5,4	10	414	3,2	2	618	1,0	6	830	7,6
3	3	3	7,6	7	211	5,4	11	415	3,2	3	619	1,0	...	...	...
4	4	4	7,6	8	212	5,4	0	416	3,2	4	620	1,0	...	...	...
5	5	5	7,6	9	213	5,4	1	417	3,2	5	621	1,0	...	...	...
6	6	6	7,6	10	214	5,4	2	418	3,2	6	622	1,0	...	...	...
7	7	7	7,6	11	215	5,4	3	419	3,2	7	623	1,0	...	...	...
8	8	8	7,6	0	204	5,4	4	408	3,2	8	612	1,0	...	...	...
9	9	9	7,6	1	205	5,4	5	409	3,2	9	613	1,0	...	...	...
10	10	10	7,6	2	206	5,4	6	410	3,2	10	614	1,0	...	...	...
11	11	11	7,6	3	207	5,4	7	411	3,2	11	615	1,0	...	...	...

Symbol	Segment 0			Segment 1			Segment 2			Segment 3			Segment 4		
	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits
12	0	0	5,4	4	208	3,2	8	412	1,0	0	624	7,6	...	...	...
13	1	1	5,4	5	209	3,2	9	413	1,0	1	625	7,6	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
19	7	7	5,4	11	215	3,2	3	419	1,0	7	631	7,6	...	...	...
20	8	8	5,4	0	204	3,2	4	408	1,0	8	632	7,6	...	...	...
21	9	9	5,4	1	205	3,2	5	409	1,0	9	633	7,6	...	...	...
22	10	10	5,4	2	206	3,2	6	410	1,0	10	634	7,6	...	...	...
23	11	11	5,4	3	207	3,2	7	411	1,0	11	635	7,6	...	...	...
24	0	0	3,2	4	208	1,0	8	420	7,6	0	624	5,4	...	...	...
25	1	1	3,2	5	209	1,0	9	421	7,6	1	625	5,4	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
31	7	7	3,2	11	215	1,0	3	427	7,6	...	...	...	...	...	...
32	8	8	3,2	0	204	1,0	4	428	7,6	...	...	...	...	...	...
33	9	9	3,2	1	205	1,0	5	429	7,6	...	...	...	...	...	...
34	10	10	3,2	2	206	1,0	6	430	7,6	...	...	...	...	...	...
35	11	11	3,2	3	207	1,0	7	431	7,6	...	...	...	...	...	...
36	0	0	1,0	4	216	7,6	8	420	5,4	...	...	...	...	...	...
37	1	1	1,0	5	217	7,6	9	421	5,4	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
47	11	11	1,0	3	227	7,6	...	...	...	...	...	...	...	...	...
48	0	12	7,6	4	216	5,4	...	...	...	...	...	...	...	...	...
49	1	13	7,6	5	217	5,4	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
95	11	23	1,0	...	...	...	...	...	...	...	...	...	...	...	...
96	0	24	7,6	...	...	...	...	...	...	...	...	...	...	...	...
97	1	25	7,6	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
767	11	191	1,0	...	...	...	...	...	...	...	...	...	...	...	...
768	0	192	7,6	...	...	...	...	...	...	...	...	...	...	...	...
769	1	193	7,6	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
815	11	203	1,0	3	419	7,6	7	623	5,4	11	827	3,2	...	...	...
816	0	204	7,6	4	408	5,4	8	612	3,2	0	816	1,0	...	...	...
817	1	205	7,6	5	409	5,4	9	613	3,2	1	817	1,0	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
827	11	215	7,6	3	419	5,4	7	623	3,2	11	827	1,0	...	...	...

5.3 Synchronization

Synchronization of the 8-VSB signal comprises Data Segment synchronization and Data Field synchronization.

5.3.1 Data Segment Sync

The encoded trellis data shall be passed through a multiplexer that inserts the various synchronization signals (Data Segment Sync and Data Field Sync).

A two-level (binary) 4-symbol Data Segment Sync shall be inserted into the 8-level digital data stream at the beginning of each Data Segment. (The MPEG-2 sync byte shall be replaced by Data Segment Sync.) The Data Segment Sync embedded in random data is illustrated in Figure 5.8.

A complete segment shall consist of 832 symbols: 4 symbols for Data Segment Sync, and 828 data plus parity symbols. The Data Segment Sync shall consist of four symbols of level +5 or –5 in the pattern (+5, –5, –5, +5) as shown in Figure 5.8. The same sync pattern occurs regularly at ~ 77.3 µs intervals, and is the only signal repeating at this rate. Unlike the data, the symbols for Data Segment Sync are not Reed-Solomon or trellis encoded, nor are they interleaved.

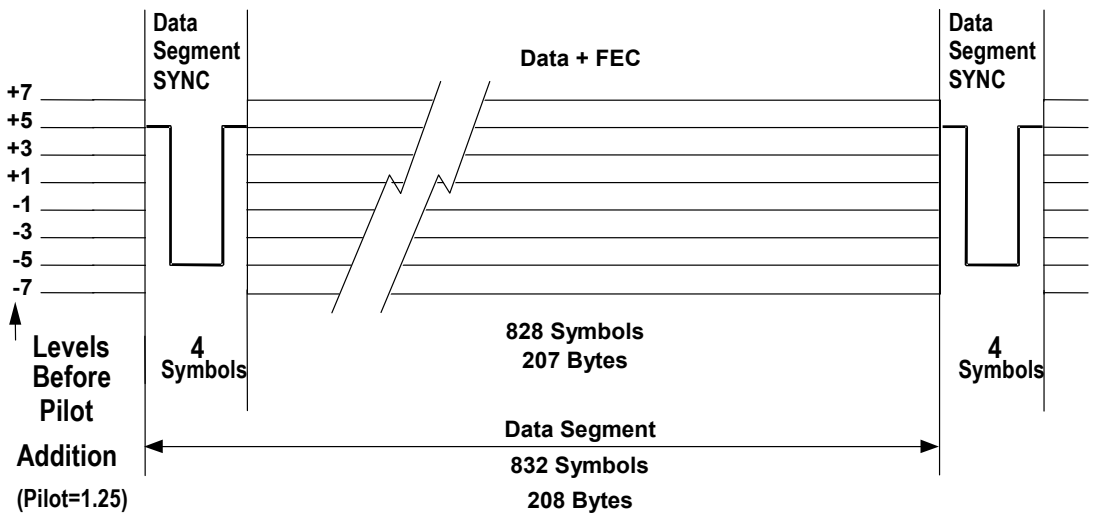


Figure 5.8 8-VSB Data Segment.

5.3.2 Data Field Sync

The data are not only divided into Data Segments, but also into Data Fields, each consisting of 313 segments. Each Data Field (~24.2 ms) shall start with one complete Data Segment of Data Field Sync, as shown in Figure 5.9. The arrangement of the 832 symbols in the Data Field Sync is defined below. Refer to Figure 5.9 for the placement of these components during the Data Field Sync. The Data Field Sync begins with a Data Segment Sync as defined in Section 5.3.1.

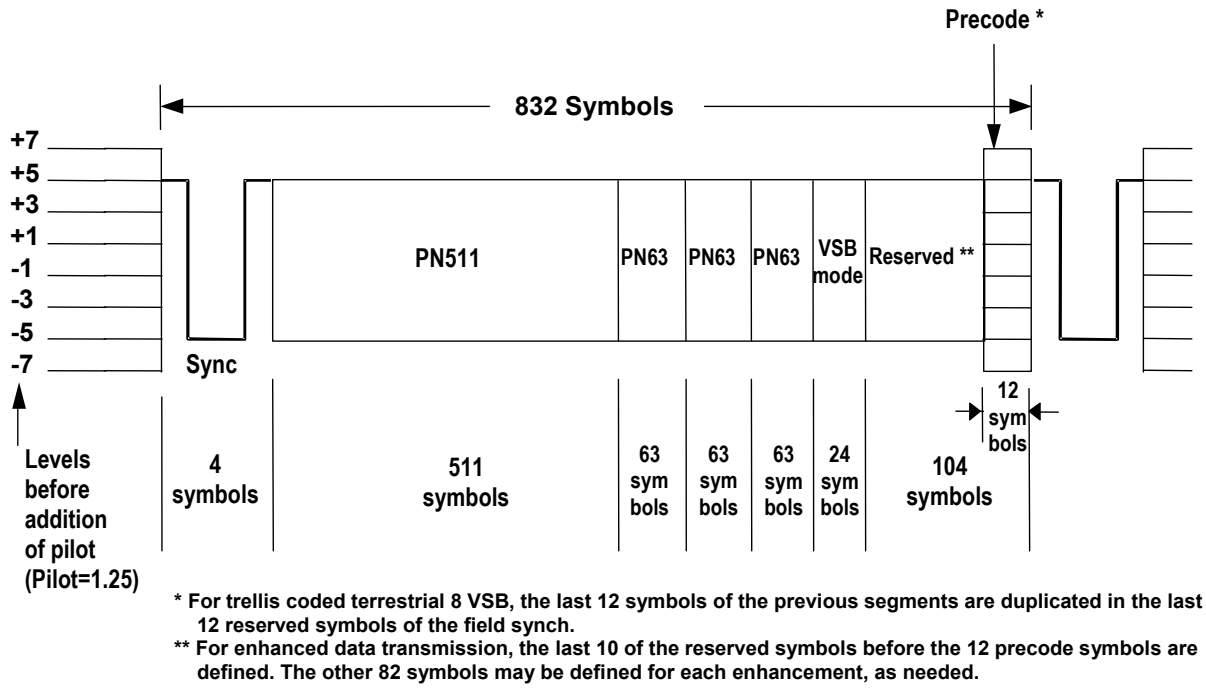


Figure 5.9 VSB Data Field Sync.

5.3.2.1 Definition of the PN511 Sequence

The Data Segment Sync shall be followed by a 511-symbol pseudo-random (PN511) sequence (see Figure 5.9). This pseudo-random sequence shall be generated from the expression $X^9 + X^7 + X^6 + X^4 + X^3 + X + 1$ with a pre-load value of '010000000' (see Figure 5.10). The resulting sequence is:

'0000 0001 0111 1111 1100 1010 1010 1110 0110 0110 1000 1000 1001 1110 0001 1101
0111 1101 0011 0101 0011 1011 0011 1010 0100 0101 1000 1111 0010 0001 0100 0111
1100 1111 0101 0001 0100 1100 0011 0001 0000 0100 0011 1111 0000 0101 0100 0000
1100 1111 1110 1110 1010 1001 0110 0110 0011 0111 0111 1011 0100 1010 0100 1110
0111 0001 0111 0100 0011 0100 1111 1011 0001 0101 1011 1100 1101 1010 1110 1101
1001 0110 1101 1100 1001 0010 1110 0011 1001 0111 1010 0011 0101 1000 0100 1101
1111 0001 0010 1011 1100 0110 0101 0000 1000 1100 0001 1110 1111 1101 0110 1010
1100 1001 1001 0001 1101 1100 0010 1101 0000 0110 1100 0000 1001 0000 0001 110'

A binary value of '1' shall be indicated by a symbol of level +5 and a binary value of '0' shall be indicated by a symbol of level –5.

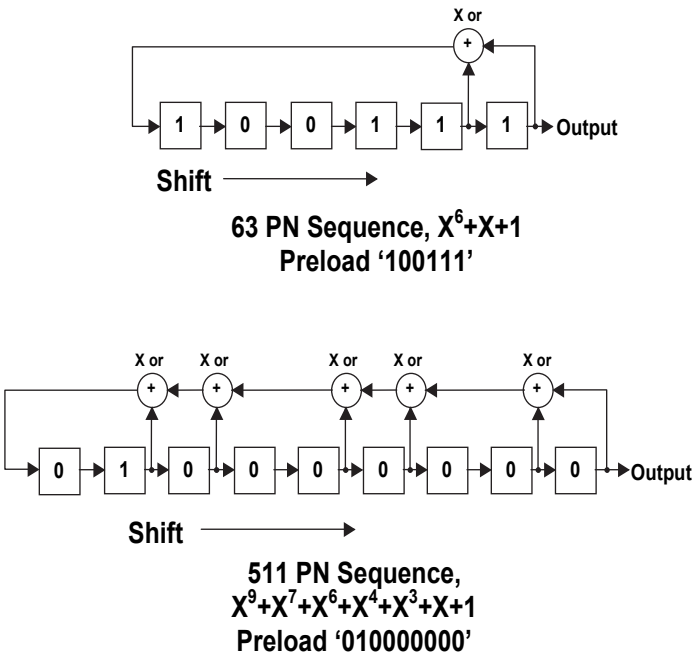


Figure 5.10 Field sync PN sequence generators.

5.3.2.2 Definition of the PN63 Sequence

The PN511 shall be followed by three 63-symbol pseudo-random (PN63) sequences (see Figure 5.9). Each pseudo-random sequence shall be generated from the expression $X^6 + X + 1$ with a pre-load value of '100111' (see Figure 5.10). The resulting PN63 sequence is:

'1110 0100 1011 0111 0110 0110 1010 1111 1100 0001 0000 1100 0101 0011 1101 000'

The middle PN63 shall be inverted on every other Data Field Sync. A binary value of '1' shall be indicated by a symbol of level +5 and a binary value of '0' shall be indicated by a symbol of level –5.

5.3.2.3 VSB Mode Bits

The VSB Mode symbols shall follow the third occurrence of the PN63 sequence. These 24 symbols shall signal the VSB mode for the data in the associated Data Field. The values of these symbols shall be determined by the values of the VSB mode bits as defined in Table 5.3. A binary value of '1' shall be indicated by a symbol of level +5 and a binary value of '0' shall be indicated by a symbol of level –5.

Table 5.3 VSB Mode Bit Definitions

Bit pattern[1] First Byte	Second Byte	Third Byte	**Mode**[2]
0000 1111	0000 1111	0000 1111	2 VSB (prohibited in A/53-defined systems)
0000 1111	0000 1111	1001 0110	4 VSB (prohibited in A/53-defined systems)
0000 1111	0000 1111	1010 0101	8 VSB (non-trellis-coded) (prohibited in A/53-defined systems)
0000 1111	0000 1111	0011 1100	Prohibited in both A/53-defined systems and in ITU J.83
0000 1111	0000 1111	1100 0011	16 VSB
0000 1010	0101 1111	0101 1010	8 VSB (trellis coded)
0000 1111	0000 1111	0110 1001	Prohibited in both A/53-defined systems and in ITU J.83
0000 1111	0000 1111	1111 0000	Prohibited in both A/53-defined systems and in ITU J.83

Notes:

1: The value of the third byte is derived from the pattern:

$$P\ A\ B\ C\ \overline{P\ A\ B\ C}$$

where A, B, C are mode bits and P is the even parity value of the mode bits. The first two bytes have the same specified pattern for all modes except for the 8 VSB trellis coded mode, where the first two bytes are derived from the pattern:

$$0\ 0\ 0\ 0\ \overline{P\ A\ B\ C\ P\ A\ B\ C}\ 1\ 1\ 1\ 1$$

2: Modes other than 16 VSB and 8 VSB (trellis coded) are defined in ITU-T J.83 [6] and are included for information only.

A binary value of ‘1’ shall be indicated by a symbol of level +5 and a binary value of ‘0’ shall be indicated by a symbol of level –5.

5.3.2.4 Reserved

In the 8-VSB mode, 92 symbols of the last 104 symbols shall be reserved, and they shall be followed by the 12 symbols defined below. To maintain a longer period with a flat spectrum, it is recommended that these 92 symbols be filled with a continuation of the PN63 sequence when only 8-VSB is present.

When one or more enhanced data transmission methods are used, the previously reserved symbols (including the 12 precode symbols) shall be numbered from 1 to 104, in the order transmitted. The 12 precode symbols shall be preceded by 10 symbols that shall be used to signal the presence of an enhancement or enhancements, as defined below. The use of some or all of the remaining 82 symbols shall be defined by each enhancement.

5.3.2.5 Precode

In the 8 VSB mode, the last 12 symbols of the segment shall correspond to the last 12 symbols of the previous segment. All sequences are pre-loaded before the beginning of the Data Field Sync.

Like the Data Segment Sync, the Data Field Sync is not Reed-Solomon or trellis encoded, nor is it interleaved.

5.3.2.6 Enhancement Signaling

Symbols 83 through 92 shall be used for indication of future enhancements. The state of each symbol shall be used to indicate the value of a bit; the combination of the bit values shall indicate the enhancements employed and/or certain characteristics of those enhancements. For convenience of representation, the bits shall be identified by numbers corresponding to the symbols that carry their values.

Bits having the value 0 shall be indicated by corresponding symbols having the level –5 during odd data fields (i.e., those fields having a non-inverted PN63 sequence within the preceding structure) and +5 during even data fields (i.e., those fields in which the preceding PN63 sequence is inverted). Bits having the value 1 shall be indicated by corresponding symbols having the level +5 during odd data fields and the level –5 during even data fields.

Bits (and, hence, symbols) 83 and 84 (called "Context Bits") shall be used to indicate the context of the remaining bits and their corresponding symbols (i.e., bits/symbols 85 through 92, called "Enhancement Bits"). The values of the Context Bits indicate which of four possible sets of meanings for the values of the Enhancement Bits is to be applied. Table 5.4 lists the values of the Context Bits and the Context Numbers that they indicate.

Table 5.4 Context Bits related to Context Numbers

Bit 83	Bit 84	Context Number
0	0	0
0	1	1
1	0	2
1	1	3

Specific meanings of the Enhancement Bits with respect to the enhancements that they signal shall be provided in other documents that reference this document and this subsection. Those other documents shall specify both the applicable Context Number and the meanings of the Enhancement Bits that they define. For each Context Number, there shall be only one definition for each of the Enhancement Bits. Undefined Enhancement Bits shall be set to a value of 0. It shall be permissible, within a single context, to signal simultaneously the existence of multiple enhancements or multiple enhancement characteristics in the transmitted signal. The condition of no enhancements being transmitted shall be signaled by Context Number 0 and all of the Enhancement Bits having a value of 0.

5.4 Modulation

The 8-level symbols combined with the binary Data Segment Sync and Data Field Sync signals are used to suppressed-carrier modulate a single carrier. The lower sideband is removed except for a small transition region. A linear-phase, root-raised cosine Nyquist filter response is employed for spectral shaping in the transmitter. This results in a spectral response that is essentially flat except for the transition regions at each end, as shown in Figure 5.11.

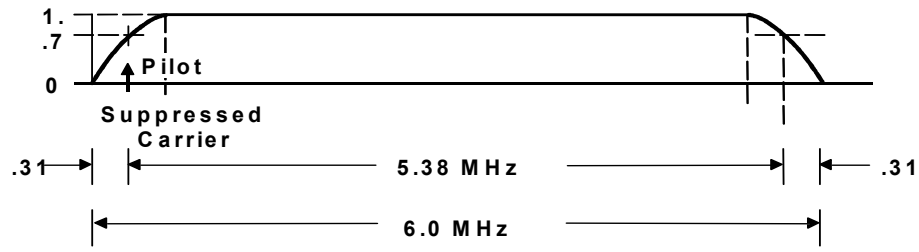


Figure 5.11 VSB channel occupancy (nominal).

In the concatenated transmitter and receiver, the resulting transition regions have a raised cosine shape as shown in Figure 5.12

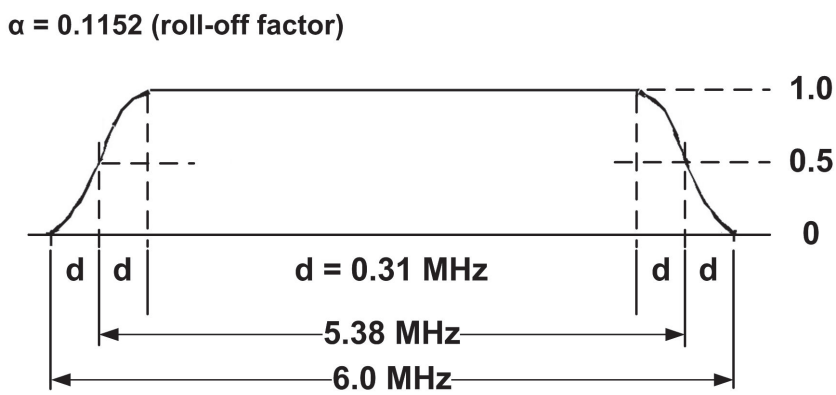


Figure 5.12 Overall VSB transmitter plus receiver linear amplitude response versus frequency (concatenation of linear-phase root-raised cosine Nyquist filters).

5.4.1 Bit-to-Symbol Mapping

Figure 5.6 shows the mapping of the outputs of the trellis encoder to signal levels of (–7, –5, –3, –1, 1, 3, 5, 7). As shown in Figure 5.8, the levels of Data Segment Sync and Data Field Sync are –5 and +5.

5.4.2 Pilot Addition

After the bit-to-symbol mapping and insertion of Data Segment Sync, a small pilot at the suppressed-carrier frequency (nominally 309 kHz from the lower band edge) and in-phase with the suppressed carrier shall be added to the signal, equivalent to a DC level of 1.25 added to every symbol (data and sync) of the digital baseband data plus sync signal (having levels of ±l,

±3, ±5, ±7 before addition of the pilot).[4] The resulting power of the pilot is approximately 11.3 dB below the average data signal power.

5.4.3 8-VSB Modulation Method

The symbols with added pilot (as described in Section 5.4.2) shall suppressed-carrier modulate a single carrier. The VSB modulator shall use the 10.76 Msymbols/s, 8-level trellis encoded composite data signal (pilot and sync added). Nominally, the roll-off in the transmitter shall have the response of a linear-phase root-raised cosine filter with α (roll-off factor) equal to 0.1152.

6. TRANSMISSION CHARACTERISTICS FOR HIGH DATA RATE MODE

6.1 Overview

The high data rate mode trades off transmission robustness (28.3 dB signal-to-noise threshold) for payload data rate (38.57 Mbps). Most parts of the high data rate mode VSB system are identical or similar to the terrestrial system. A pilot, Data Segment Sync, and Data Field Sync are all used to provide enhanced operation. The pilot in the high data rate mode also is 11.3 dB below the data signal power. The symbol, segment, and field signals and rates are all the same, allowing either receiver to lock up on the other's transmitted signal. Also, the data frame definitions are identical. The primary difference is the number of transmitted levels (8 versus 16) and the use of trellis coding and NTSC interference rejection filtering in the terrestrial system.

The RF spectrum of the high data rate modem transmitter looks identical to the terrestrial system, as illustrated in Figure 5.11. Figure 6.1 illustrates a typical Data Segment, where the number of data levels is seen to be 16 due to the doubled data rate. Each portion of 828 data symbols represents 187 data bytes and 20 Reed-Solomon bytes followed by a second group of 187 data bytes and 20 Reed-Solomon bytes (before convolutional interleaving).

[4] The formula for determining the location of the pilot with respect to the lower edge of the theoretical occupied bandwidth is

$$\text{pilot frequency} = \left[6 - \frac{Tr \times \frac{208}{188} \times \frac{313}{312}}{4} \right] \div 2 \text{ MHz}$$

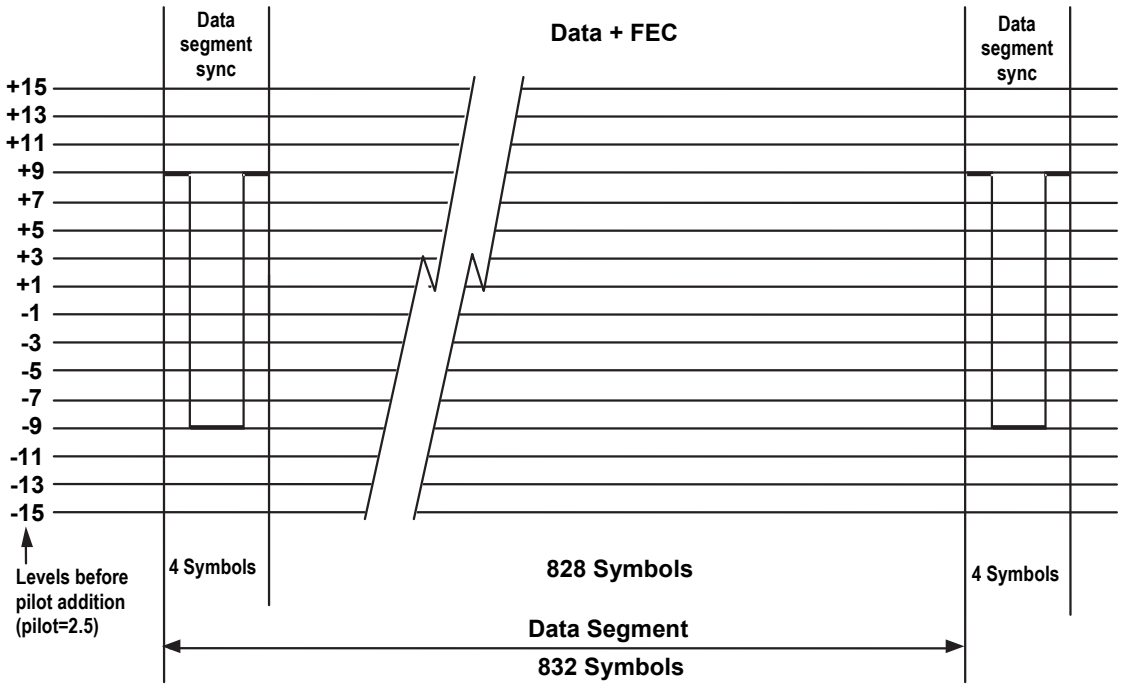


Figure 6.1 16-VSB Data Segment.

Figure 6.2 shows the block diagram of the transmitter. It is identical to the terrestrial VSB system except the trellis coding shall be replaced with a mapper that converts data to multi-level symbols. See Figure 6.3.

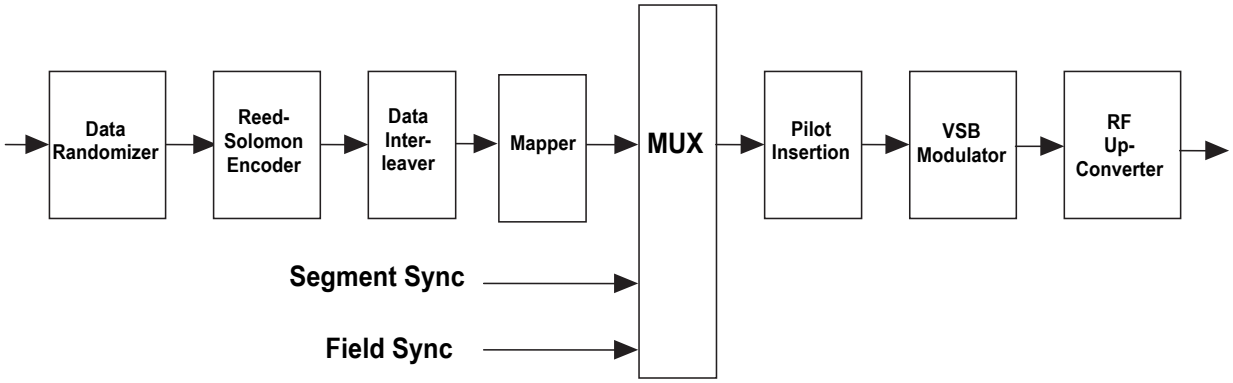
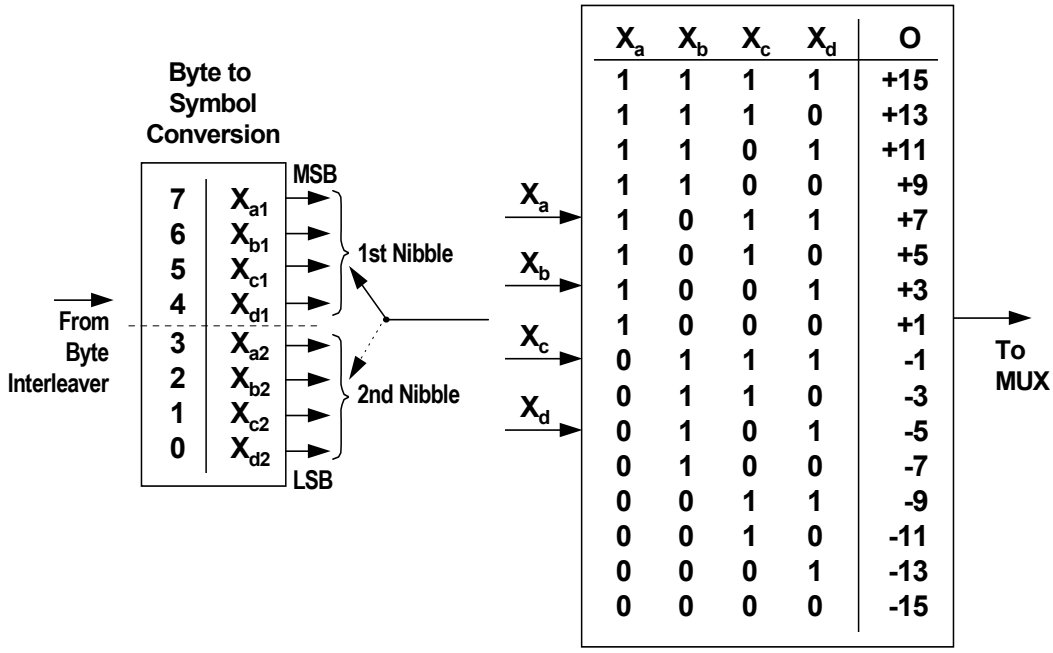


Figure 6.2 16-VSB transmitter.



X_a	X_b	X_c	X_d	O
1	1	1	1	+15
1	1	1	0	+13
1	1	0	1	+11
1	1	0	0	+9
1	0	1	1	+7
1	0	1	0	+5
1	0	0	1	+3
1	0	0	0	+1
0	1	1	1	-1
0	1	1	0	-3
0	1	0	1	-5
0	1	0	0	-7
0	0	1	1	-9
0	0	1	0	-11
0	0	0	1	-13
0	0	0	0	-15

Figure 6.3 16-VSB mapper.

6.2 Channel Error Protection and Synchronization

6.2.1 Data Randomizer

See Section 5.2.1.

6.2.2 Reed-Solomon Encoder

See Section 5.2.2.

6.2.3 Interleaving

The interleaver shall be a 26 Data Segment inter-segment convolutional byte interleaver. Interleaving is provided to a depth of about 1/12 of a Data Field (2 ms deep). Only data bytes shall be interleaved.

6.2.4 Data Segment Sync

See Section 5.3.1.

6.2.5 Data Field Sync

See Section 5.3.2.

6.3 Modulation

6.3.1 Bit-to-Symbol Mapping

Figure 6.3 shows the mapping of the outputs of the interleaver to the nominal signal levels (–15, –13, –11, ..., 11, 13, 15). As shown in Figure 6.1, the nominal levels of Data Segment Sync and Data Field Sync are –9 and +9. The value of 2.5 is added to all these nominal levels after the bit-to-symbol mapping for the purpose of creating a small pilot carrier.

6.3.2 Pilot Addition

A small in-phase pilot shall be added to the data signal. The frequency of the pilot shall be the same as the suppressed-carrier frequency as shown in Figure 5.11. This can be generated in the following manner. A small (digital) DC level (2.5) shall be added to every symbol (data and sync) of the digital baseband data plus sync signal (±l, ±3, ±5, ±7, ±9, ±11, ±13, ±15). The power of the pilot shall be 11.3 dB below the average data signal power.

6.3.3 16 VSB Modulation Method

The modulation method shall be identical to that in Section 5.4.3, except the number of transmitted levels shall be 16 instead of 8.